Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An electronic device, comprising:
an interlevel dielectric layer formed on a semiconductor substrate;
a copper bottom electrode formed in said interlevel dielectric layer, a top surface of said bottom electrode co-planer with a top surface of said interlevel dielectric layer;
a conductive diffusion barrier in direct contact with said top surface of said bottom electrode;
a MIM dielectric in direct contact with a top surface of said conductive diffusion barrier; and
a top electrode in direct contact with a top surface of said MIM dielectric.

[c2] 2. The electronic device of claim 1, wherein said conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said bottom electrode.

[c3] 3. The electronic device of claim 1, further including:
a dielectric diffusion barrier layer formed on said top surface of said interlevel dielectric layer; and
wherein said top surface of said conductive diffusion barrier is co-planer with a top surface of said dielectric

diffusion barrier layer.

[c4] 4. The electronic device of claim 1, wherein said bottom electrode includes an upper portion comprising an additional conductive diffusion barrier, said upper portion in contact with said conductive diffusion barrier.

[c5] 5. The electronic device of claim 4, wherein said additional conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

[c6] 6. The electronic device of claim 1, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

[c7] 7. The electronic device of claim 1, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations of layers thereof.

[c8] 8. The electronic device of claim 1, wherein said top electrode comprises Al or W.

[c9] 9. An electronic device, comprising:
an interlevel dielectric layer formed on a semiconductor substrate;

a copper bottom electrode formed in said interlevel dielectric layer;

a conductive diffusion barrier in direct contact with a top surface of said bottom electrode, said top surface of said bottom electrode recessed below a top surface of said interlevel dielectric layer, said top surface of said conductive diffusion barrier co-planer with said top surface of said interlevel dielectric layer;

a MIM dielectric in direct contact with a top surface of said conductive diffusion barrier; and

a top electrode in direct contact with a top surface of said MIM dielectric.

[c10] 10. The electronic device of claim 9, wherein said conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said bottom electrode.

[c11] 11. The electronic device of claim 9, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

[c12] 12. The electronic device of claim 9, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

[c13] 13. The electronic device of claim 9, wherein said top electrode comprises Al or W.

[c14] 14. A method of fabricating an electronic device, comprising:

(a) providing a semiconductor substrate

(b) forming an interlevel dielectric layer on said semiconductor substrate;

(c) forming a copper bottom electrode in said interlevel dielectric layer, a top surface of said bottom electrode co-planer with a top surface of said interlevel dielectric layer;

(d) forming a conductive diffusion barrier in direct contact with said top surface of said bottom electrode;

(e) forming a MIM dielectric in direct contact with a top surface of said conductive diffusion barrier; and

(f) forming a top electrode in direct contact with a top surface of said MIM dielectric.

[c15] 15. The method of claim 14, wherein said conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said bottom electrode.

[c16] 16. The method of claim 14, further including:

(g) after step (c) forming a dielectric diffusion barrier layer on said top surface of said interlevel dielectric layer; and

wherein said top surface of said conductive diffusion barrier is co-planer with a top surface of said dielectric diffusion barrier layer.

[c17] 17. The method of claim 14, wherein said bottom electrode includes an upper portion comprising an additional conductive diffusion barrier, said upper portion in contact with said conductive diffusion barrier.

[c18] 18. The method of claim 17, wherein said additional conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

[c19] 19. The method of claim 14, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

[c20] 20. The method of claim 1, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

[c21] 21. The method of claim 14, wherein said top electrode comprises Al or W.

[c22] 22. The method of claim 14, wherein step (d) further

comprises simultaneously forming a resistor, an alignment mark or both a resistor and an alignment mark with said conductive diffusion barrier.

[c23] 23. The method of claim 22, wherein said resistor, said alignment mark or both said resistor and said alignment mark comprise about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations of layers thereof.

[c24] 24. The method of claim 14, further including (g) after step (f) depositing a reactive ion etch layer over all exposed surfaces of said conductive diffusion barrier, said MIM dielectric and said interlevel dielectric layer.

[c25] 25. A method of fabricating an electronic device, comprising:

(a) providing a semiconductor substrate;

(b) forming an interlevel dielectric layer on said semiconductor substrate;

(c) forming a copper bottom electrode in said interlevel dielectric layer;

(d) forming a conductive diffusion barrier in direct contact with a top surface of said bottom electrode, said top surface of said bottom electrode recessed below a top surface of said interlevel dielectric layer, said top surface of said conductive diffusion barrier co-planer with said

top surface of said interlevel dielectric;

(e) forming a MIM dielectric in direct contact with said top surface of said conductive diffusion barrier; and

(f) forming a top electrode in direct contact with a top surface of said MIM dielectric.

[c26] 26. The method of claim 25, wherein said conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said bottom electrode.

[c27] 27. The method of claim 25, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

[c28] 28. The method of claim 25, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

[c29] 29. The method of claim 25, wherein said top electrode comprises Al or W.

[c30] 30. The method of claim 25, further including (g) after step (f) depositing a reactive ion etch layer over all exposed surfaces of said conductive diffusion barrier, said MIM dielectric and said interlevel dielectric layer.